DfX – Design for Excellence

How to build a consistent 'design-to-test' flow in order to deliver defect-free PCBA's

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ABSTRACT

Design for Excellence (DfX) can be used as part of an organization's Continuous Improvement Programme to decrease product development time, product cost and manufacturing cycle time, while increasing product quality, reliability and ultimately the customer satisfaction.
It will significantly decrease the overall cycle time from the design concept to customer delivery, which is a critical success factor.
Design for Excellence makes it possible to implement a Lean Test approach that produces a lower cost product whilst maintaining the highest quality.

ASTER's vision is articulated on two principles: ❶ Using traceability and repair loop information in order to qualify the customer defect universe. The defects include design defects, manufacturing defects and functional defects. ❷ Importing the defect opportunities and identifying the possible consequences of inadequate testability and test coverage on a new design.

INTRODUCTION

Traditionally, manufacturing and test constraints are only considered at the end of the layout phase, prior to transfer of the CAD data to production. Due to board complexity, it is now mandatory to consider a validation stage at each step of the design and manufacturing phases.

TestWay has been developed to allow users to analyze each stage of the design to delivery workflow.

This is achieved by the following stages:

- **Design for Component** – When the key components are selected, check the ROHS, reliability, defects per million opportunities (DPMO), boundary-scan description language (BSDL) file validation in order to guide component selection.
- **Electrical Design for Test** – When the schematic sheets are defined, verify the testability by conducting electrical rules checking that reflect the Design for Test (DfT) guide lines.
  These can include standard and customer's specific checks relating to company requirements.
  By simulating the test strategy prior to the layout phase, helps to minimize the need for physical accesses that are necessary to detect defects aligned to the defect universe. It helps to reduce test point access by 30% to 70%!
- **Mechanical Design for Test** – When the layout is finalized, test probe placement should be optimized according to test strategy definitions. The probe access information can then be used for estimating the test coverage, modeling the cost and calculating the production yield and TL9000 initial return rates.

- **Design to Build and Design to Test** – It is key to estimate test coverage using theoretical models that reflect the capabilities for a wide range of test and inspection strategies, such as:
  Automated Placement Machines (APM);
  Automatic Optical Inspection (AOI);
  Automated X-ray Inspection (AXI);
  Boundary-scan Test (BST);
  Flying-probe Test (FPT);
  In-Circuit Test (ICT) and Functional Test

  These models should be tuned to reflect the test and measurement capabilities of each individual target tester.

  It is also beneficial to export CAD data in the native format useable by Assembly machines, Automated Optical Inspection, Automated X-Ray, In-Circuit testers, Flying-probe testers and Boundary-Scan testers that is aligned to the simulated strategy.
  The exported files may include assembly and test programs, input lists, test models, as well as test fixture files used by the target testers.
  Any files created at the Design to Test stage can significantly reduce the downstream test development and fixturing costs.
- **Test for Excellence** – Once the test and inspection programs have been debugged and released, it is imperative to be able read the completed test program or test report and compare the coverage between the estimated and measured analysis. By analyzing the true coverage, test coverage analysis reports can be created to reflect what is actually being tested.
  Industry standard metrics should be used in the coverage analysis so that it is possible to make direct comparisons and identify any misalignment between the estimated and real coverage. So that any test escapes are identified and rectified prior to main stream production.
  Quality traceability tools used in the diagnosis and repair of printed circuit boards can take advantage of detailed test coverage analysis to improve the diagnostic resolution and speed up the repair process.
- **Test for Designability** – Test is an important contributor for design improvement, once a feedback loop between production and design has been established, such as a concurrent engineering approach to design and test.

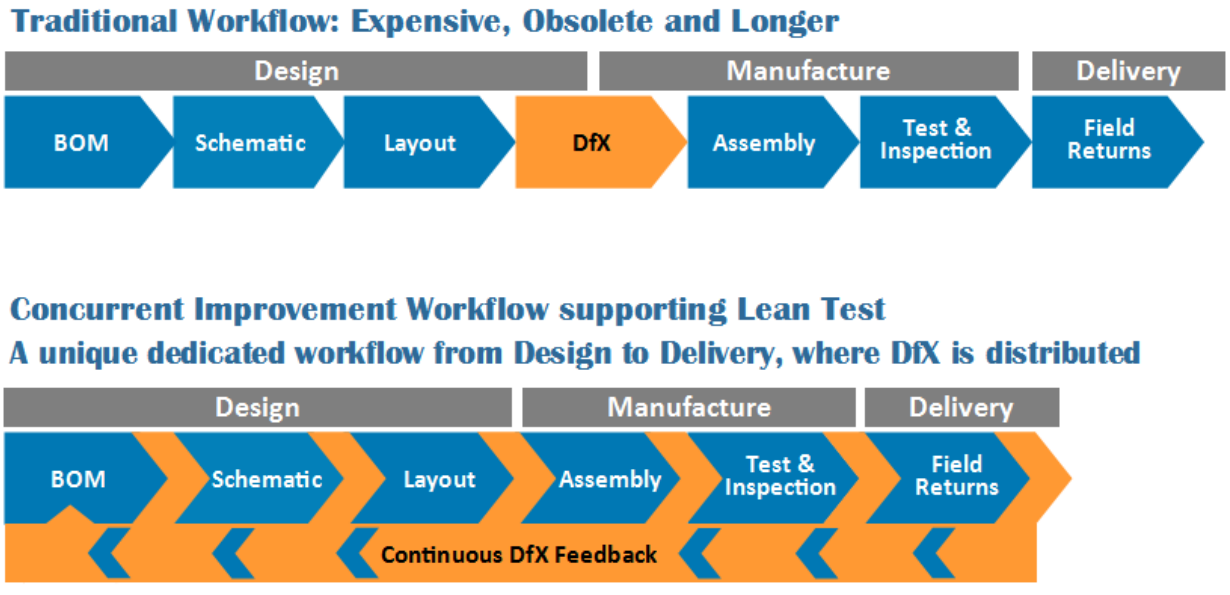

Fig.1 Current Improvement Workflow with distributed Design for Excellence (DfX)

DFX WORKFLOW

The DfX workflow requires continuous assessment at each stage in the Design to Delivery process, with feedback provided at each stage in the process.
It is imperative to verify adequate DfT at schematic prior to committing to layout to ensure that testability issues are resolved prior to manufacture.

Companies must deliver good products to their customers; defect free and at minimum cost.
The challenge is how to detect, or prevent defects from occurring, so that only good products are shipped to the customer.

A tested Printed Circuit Board Assembly (PCBA) cannot be assumed to be good and free of defects, simply because the test passes.
Test coverage is a key metric since it is the measurement that warrants the product quality and is the main driving factor in creating a lean test strategy.

Design data must be analyzed at the earliest stage in the product life cycle by importing schematic netlist data.
So that electrical design or DfT violations are identified and rectified prior to commitment for board layout, preventing costly design re-spins.

Traditional commercial DfX tools work only from the layout stage, which is often too late in the design process to be of use.

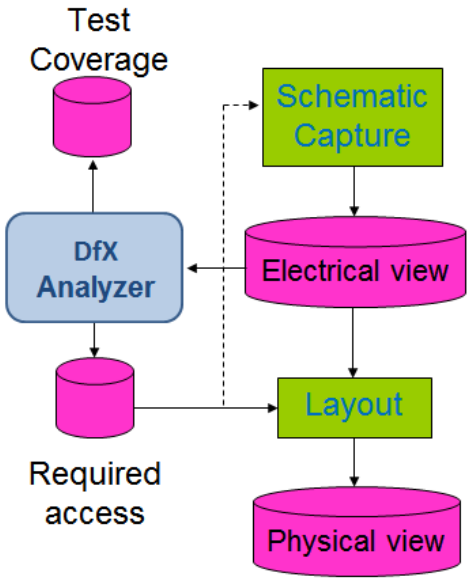

Fig.2 Schematic – Electrical DfT

Test point optimization can be provided pre-layout during the schematic capture stage. Thus reducing the need for unnecessary test access and saving on PCB real estate, particularly on high density boards.

Design and testability rules violations limit the test coverage. Subsequently it is imperative that accessibility is assessed prior to layout in alignment with the test strategies that will be used during manufacturing.
Once the PCBA board layout is completed, a mechanical DfT analysis must be conducted to determine whether there is adequate test access after all the mechanical probing constraints have been considered.
It is possible that some access will be lost because probe access is too close to the body of a component, or probes are too close together etc.

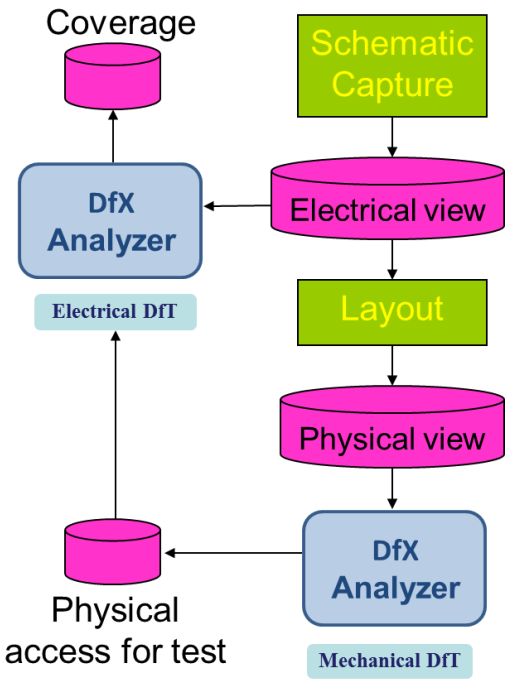

Fig.3 Layout - Mechanical DfT

It is also important to consider further savings to be made, such as when a fixture is designed for PCBA test purposes; there are limitations on nail sizes and possible probe positions. Future proofing and reliability of the fixture should be considered against modifications to the PCBA design. Larger nail sizes are generally more reliable and smaller nails are required for accessing densely populated designs.

Test development savings can also be made during the test program debug phase. It can be time consuming hunting through sheets of schematics and product related documents in order to produce a working test.
The process can be simplified by automatically assessing the board topology and design connectivity, reporting directly on components where the chosen test strategy is not adequate to identify potential faults.

Once the gaps in test coverage are identified, alternative complementary test strategies can be considered, or existing test strategies improved to plug the gaps.

TEST COVERAGE

For an absurd example on how test coverage is calculated.
Let us consider a simple PCBA comprising of 4 components: 3 resistors and 1 BGA.

The 3 resistors are measured with very high accuracy, but there is no test on the BGA.
So is the board test score really 75%?

3 resistors / 4 components

Clearly it is not. So we need something to weight the test coverage, which is credible and can be easily updated to reflect the growing electronics complexity.

If we are to consider all the manufacturing defects within the defect universe such as: missing components; wrong value; misalignment; incorrect polarity; damaged components; open circuits; short circuits; insufficient solder and excessive solder.

We must have test strategies in place that are capable of detecting these defects.
The ability to detect defects can be expressed by a coverage facet, so that each defect category is aligned with coverage metrics.

MPSF	PPVSF	PCOLA/SOQ /FAM
Material	Value	Correct
		Live
Placement	Presence	Presence
		Alignment
	Polarity	Orientation
Solder	Solder	Short
		Open
		Quality
Function	Function	Feature
		At-Speed
		Measure

Fig.4 Test Coverage Metrics

The table in Figure.4 details industry standard metrics that have been defined by Philips Research (MPSF); ASTER Technologies (PPVSF); Agilent (PCOLA/SOQ/FAM).

These metrics allow the estimation of the theoretical coverage, or measurement of the real coverage for each unique test strategy, or combination of test strategies.
No single test strategy is capable of detecting all the defects. It is a combination of complementary test strategies that provide an overall good coverage.

When calculating test coverage it is important to consider DPMO that reflect the current manufacturing process.
This way the test coverage can be aligned such that better coverage is provided where there is a greater opportunity for defects occurring during manufacture.

In the Test Effectiveness formulae below, each defect category is associated with its corresponding coverage.

$$\text{Effectiveness} = \frac{\Sigma D_M \times C_M + \Sigma D_P \times C_P + \Sigma D_S \times C_S + \Sigma D_F \times C_F}{\Sigma D_M + \Sigma D_P + \Sigma D_S + \Sigma D_F}$$

Fig.5 Test Effectiveness

TEST ESCAPES

If a PCBA is failing at system test it is usually because the escape rate (or slip) is higher than expected.
There are two possible reasons why this situation occurs:

1. The combined coverage is lower than optimal.
2. The DPMO figures are higher than expected.

The unexpected low coverage could be due to the use of inadequate coverage metrics, such as the confusion between test accessibility and testability.
Alternatively, low coverage could be a result of only considering coverage by component presence without taking into account solder joint figures, or over optimistic reporting that is more marketing driven than providing realistic results.

Incorrect DPMO figures are probably due to limited defect traceability, or incorrect root cause analysis.
Such as a misunderstanding of the fault message provided by the fault ticket and the defect root cause assessment.

We can only improve on what can be measured.
By obtaining a reference point from early coverage estimation and comparing this with the coverage provided by the real test program running on the shop floor. It is possible to identify deviations in order to provide continuous improvements.

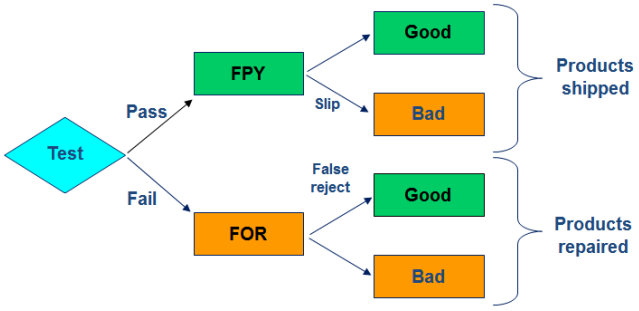

Fig.6 Production Test Model

TEST DEVIATIONS

An example of where disparity can occur between the expected test coverage and the achieved test coverage, is where the test development and PCBA manufacturing is outsourced.

The original equipment manufacturer (OEM) because of limited test engineering resources may decide to outsource the test development and manufacture to a contract manufacturer anywhere in the world, depending on price.

The contract manufacturer may not have the test capability, or knowledge to develop a test program for the target ICT machine that meets the expectations of the OEM.
The completed post debug test program should reflect the estimated coverage requirements defined by the OEM.

It is imperative that the OEM has complete visibility of what is achieved by their supplier. Otherwise there is a good chance that an inferior product could be manufactured and shipped to the end customer, which could ultimately result in lost orders, or something more serious.

The example below shows how the outsourced test program can be measured and compared against the early estimation in order to verify that the original requirements have been realized.

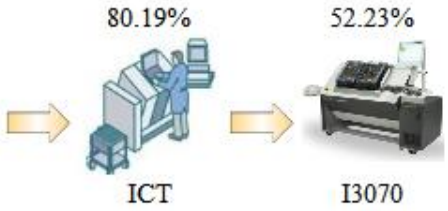

Fig.7 Comparison between estimated ICT coverage and measured Keysight i3070 coverage

COST OF TEST

The purpose of any test solution is to maximize test coverage, ensuring that all defects are detected, whilst minimizing test cost.

If you do not test a product enough you can get a reputation for poor quality products. If you test too much you could negatively impact a wide variety of business processes, include time to market and ship to target.
The manufacturing test process is an expense that is used to reduce the cost of quality issues that poses a risk to the customer experience[1].
The net result is to improve product quality, but by spending less money.

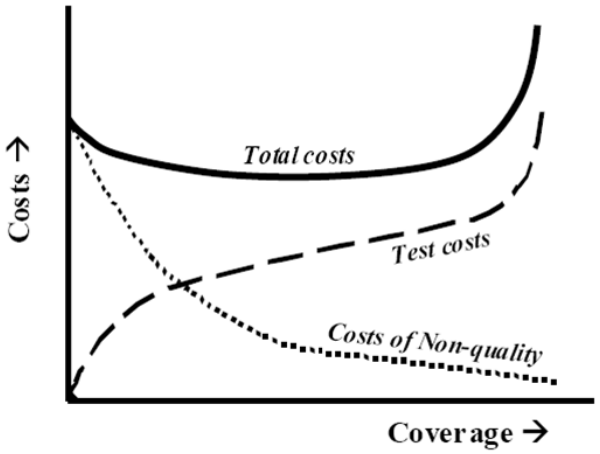

Fig.8 Cost of Test[1]

Detection of all theoretically possible defects has severe implications on test time and results in prohibitive development costs. For example, an instruction set test for a processor mounted on a board requires a significantly high investment without comparison related to the manufacturing defects.

Manufacturing tests have to target detection of probable defects (inherent to the process). This approach is named “Process Oriented Test”; as opposed to the “Product Oriented Test”[2].

Test strategy and defect occurrences should be linked together so that improved test coverage can be targeted towards defects that occur frequently. A lack of coverage on defects that never occur has no real bearing on the final product quality.

It is necessary to go beyond solving surface issues and qualify the product test strategies against the real DPMO.

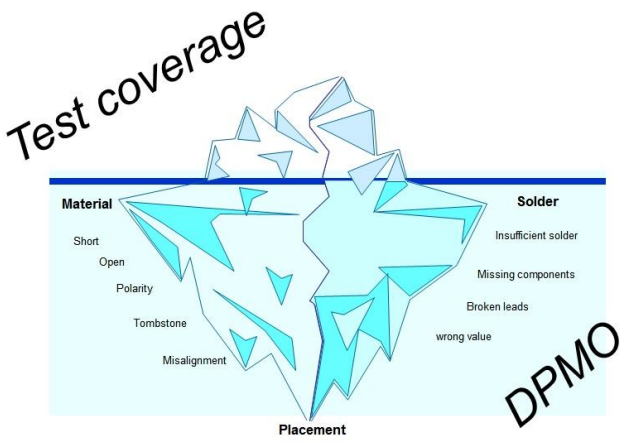

Fig.9 DPMO Extraction

CONCLUSION

Technological development produces new problems that call for new tools. Test coverage estimation is one of these tools. From design, during production, and in a more general way, through the whole product life cycle, coverage estimation permits the test process to be optimized.

In assessing the results from a combination of test methods it is possible to simulate a variety of test strategies and predict the relative fault coverage[3].
By deploying various testers in the optimum order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels improved.

The economic challenges are critical; the tools to meet them are available.

REFERENCE

[1] System manufacturing test cost model: David Williams, Anthony P. Ambler; International Test Conference, 2002.

[2] JTAG-centric board testing demands Early Design: Graham Prophet, EDN Europe, 2002.

[3] Board Defect Coverage Analysis *(From design to production)*: Christophe LOTZ; DATE 2004, Paris.