

FUNCTIONAL BOARD TEST - COVERAGE ANALYSIS

what does it mean when a functional test passes?

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Abstract

Test coverage is a key qualification tool for driving schematic design, board layout and test program development for enabling the best production yield.

A number of different test coverage models ranging from MPS to PCOLA/SOQ and PPVS have been developed in defining how the coverage metric is calculated using different fault models.

These test coverage models have been invariably used to determine the level of test coverage using structural test strategies, such as AOI, AXI, FPT, ICT, and Boundary-Scan. This paper will discuss the contribution of functional board test (FT) strategy to detect structural defects in production and as a strategy to validate the design or the function.

1 Introduction

Test coverage calculations for printed circuit boards (PCB) are becoming increasingly important as a key indicator in determining the quality of a product.

In the majority of cases PCB structural test strategies that include test and inspection techniques such as automated optical inspection (AOI), automated X-ray inspection (AXI), in-circuit test (ICT), flying probe test (FPT), and boundary-scan test (BST) are perfectly adequate in detecting the majority of manufacturing structural faults.

However, there are situations where the optimum test coverage is not achievable through structural testing, or it may be that the current test strategy provides inadequate structural test coverage due to limited access.

Under these circumstances, it may be beneficial to predict the test coverage contribution provided by functional board test (FT) to detect structural defects, not only during production but also during the product maintenance phase.

2 Manufacturing Faults

The manufacturing process is not free from introducing faults, due to the capabilities of the equipment and the process used.

Typically, the defect universe comprises of the following defect categories:

- Missing devices
- Wrong value, 10K instead of 100K
- A dead device e.g. ESD damaged or cracked device
- Incorrect polarity, rotated 180 degrees
- Device misalignment
- Tombstone effect
- Broken lead
- Short between adjacent pins caused by solder bridge, bent pins, or mis-registration
- Open solder joint
- Poor solder joint, due to excessive, insufficient or malformed solder

Subsequently it is important to categorize these faults in relationship to a group of test coverage facets that provides a logical link with the production process, and allow the model to be clearly understood by designers, project management and production people.

These test coverage facets are defined by three accepted de-facto standards for modelling test coverage, namely:

MPS	- Philips Research ¹
PPVS	- ASTER Ingénierie ²
PCOLA/SOQ	- Agilent Technologies ³

The list of faults described within the defect universe can be further sub categorized as:

- **Defects** – that can be detected by a test, or fixed by a repair.
- **Deviations** – that can be located by inspection and are fixed by process tuning.

For example the [A] Alignment and [Q] Quality facets described in the PCOLA/SOQ model are deviations in the production process that can be resolved by fine tuning the process.

However, if the deviation becomes problematic enough, it becomes a defect. The problem then becomes, how to determine at what point the deviation becomes important, which is one of the fundamental reasons for the false reject scenario with inspection tools.

2.1 Defect Universe

It is important to understand how the defects defined in the ‘defect universe’, correlate to the individual facets within each of the test coverage models. This will help to understand the reasoning in predicting the test coverage for a functional board test strategy.

This list of defects must comprise of manufacturing faults that are recognized consistently throughout the electronics industry and accepted as ‘the defect universe’ for providing a framework for test coverage metrics.

Studies have been made and published in technical papers¹²³ that identify a number of ways to represent test coverage based on the concept of multiple facets.

In trying to rationalize the various test coverage models, Lotz² identified two major problems that needed resolving:

1. How many facets are necessary to represent the most complete test coverage?
2. Consolidation of the facets into a single value.

The model we will use for computing test coverage has to be consistent with the manufacturing process. It is important that the model is easy to understand for design and manufacturing engineers.

Figure 1



The manufacturing flow comprises of three stages that determine; the supply of correct materials, the correct placement of components and the soldering of components to the PCB.

The correlation between the ‘defect universe’ defined by the various models and the different test coverage facets are shown below.

Figure 2

MPS [1]	PPVS [2]	PCOLA/SOQ [3]
Material	Value	Correct Live
Placement	Presence	Presence Alignment
	Polarity	Orientation
Solder	Solder	Short Open Quality

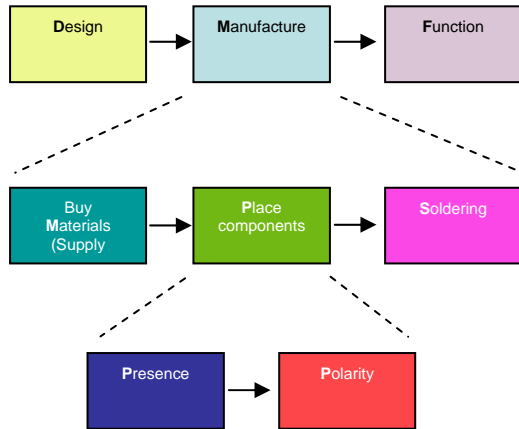
This high level (MPS) representation of the manufacturing process can be further broken down within a hierarchical tree flow to obtain lower level detail like PPVS or PCOLA/SOQ or even expanded to show additional sub-criteria:

- Absence (not fitted DNP components),
- Downloaded (Flash, FPGA, μ C),
- Component revision labeling,
- Solder shape,
- Solder density (voiding in lead-free soldering).

When functional test is considered not only as a test strategy for detecting structural defects, but also as a validation of the design function to determine that the board-under-test (BUT) is fit-for-purpose; we need 3 main defect classes:

1. **Design defects** – that have to be detected by a design rules checker (DRC), or by electrical DfT or DfM.
2. **Production defects** – MPS or PPVS model.
3. **Functional defects** – these defects are not specifically attached to a single component, but to a block of components

Figure 3



If we now take these additional defect classes into account, the test coverage model now becomes **DMPSF**.

- Design
- Material
- Placement
- Solder
- Function

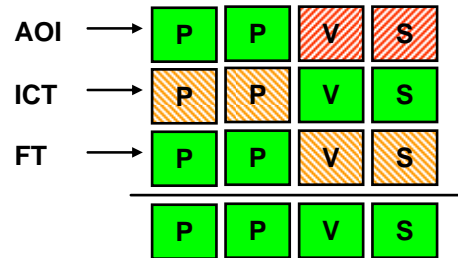
3 Complementary Test Coverage

Each test technique has the ability to detect some of the defects defined within the ‘defect universe’; however, no single solution is capable of detecting all the defects.

This can only be achieved by a combination of complimentary test techniques to provide the optimum test coverage as defined in the PPVS test coverage model.

In figure 4, we show the PPVS coverage for a combination of test techniques that comprise of structural tests; visual inspection; electrical process tests and functional (performance) tests. From this a coverage value can be predicted that represents the ability to capture all the defects.

Figure 4



3.1 Defect Opportunities

It is also important to consider in any test coverage predictions, the associated defects.

The default defect rates can be obtained either from the International Electronics Manufacturing Initiative (iNEMI) <http://www.inemi.org>, or from the Smart Group PPM (Parts Per Million) Monitoring website www.ppm-monitoring.com.

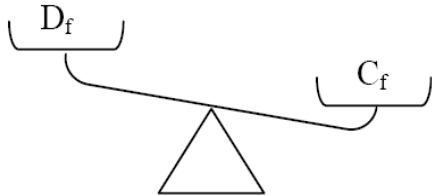
This information is useful in providing defect values based on manufacturing data obtained from industry wide PPM monitoring projects, and is particularly useful when starting the analysis on new designs and processes.

Quality management tools, such as QUAD⁴ can be used to collect the DPMO (Defects per Million Opportunities) data from local manufacturing facilities, so that yield predictions can be calculated based on real-time process data.

Taking into account DPMO data does not complete the picture, because although test coverage confirms that we can catch defects, we need to balance this with test efficiency (weighted coverage) that informs us whether the test strategy is consistent with the defect universe.

The PPVS model is based on test coverage balanced by the defects opportunities (DPMO).

Figure 5



The weighted coverage can be calculated by:

$$\text{Coverage} = \frac{\sum D_M \times C_M + \sum D_P \times C_P + \sum D_S \times C_S}{\sum D_M + \sum D_P + \sum D_S}$$

Where for each category of defects (D_f , $f \in \{M, P, S\}$), we associate the corresponding coverage (C_f , $f \in \{M, P, S\}$).

The previous formula can be further expanded to cover “Maintenance test”, where the calculation is made using the Lambda (λ) value linked to ‘failure in time’, instead of the DPMO value in production.

$$\text{Coverage} = \frac{\sum \lambda_F \times C_F + \sum \lambda_B \times C_B}{\sum \lambda_F + \sum \lambda_B}$$

Where for each category of defects (λ_f , $f \in \{F, B\}$), we associate the corresponding coverage (C_f , $f \in \{F, B\}$):

- Where *F* means component function: Failures relating to the function of the part i.e. value drift; dynamic characteristic drift; dysfunction etc. Some of these defects can be detected by ICT or BST, but functional test is more suitable.
- Where *B* means component border: Failures relating to external pins i.e. broken joints; broken bonding; defective input/output buffer etc. These defects can be detected by structural test such as ICT and BST.

A number of assumptions are considered in estimating maintenance test coverage, such as:

- Any boards shipped to the customer are considered good, so all devices are present and correct.
- When a board fails in the field it is not due to a missing or mis-orientated part.

4 Functional Test (FT)

A functional test solution is developed primarily within the hardware design environment as a test vehicle for verifying that a PCB meets its design criteria.

Once the design validation and prototyping testing phases are complete, the test vehicle is transferred to the Test Engineering department to be used as a functional test platform to verify that manufactured products meet their performance specification and are ‘fit for purpose’ to be shipped to the customer. The functional test stage is the final PCB quality gate.

However, functional testers are a challenge because:

- It is extremely difficult to predict test coverage provided by a test program unless fault simulation has been undertaken.
- Measurement statements from the test report are difficult to correlate against defects.
- Fault diagnosis is either extremely limited or in some cases non-existent, with the majority of tests simply providing PASS/FAIL status.

The estimation of the defect coverage provided by functional testing often requires far more elaborate calculations. If coverage information is available for each of the defect classes, then it makes sense to reuse this information in the functional test coverage calculations across all designs.

However, there are of course limitations in the level of defect coverage provided by functional test, as identified in the best-case analysis model presented by Nokia Networks⁵. This model clearly shows that it is not possible to predict coverage values for solder quality related defects such as:

- Insufficient solder
- Excessive solder
- Solder residue
- Granular solder joints
- Misalignment

This paper describes three methodologies to create a functional test coverage report.

1. **Declaration** – using schematic and/or layout viewers as the test coverage input device.
2. **Deduction** – from a formal test description based on customer’s rules.
3. **Inheritance** – test reuse in a hierarchical design flow where a functional block is associated with test coverage calculations.

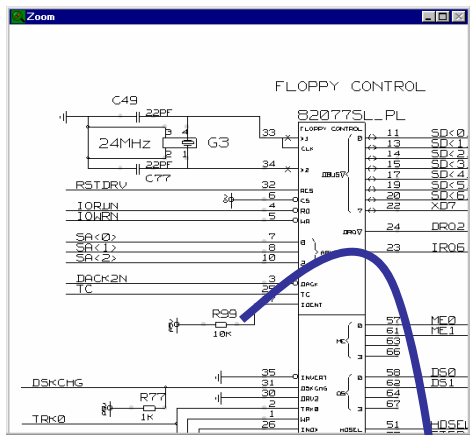
These methodologies are also applicable for system test, embedded test or stress test.

4.1 Declaration Method

The **Declaration** method utilizes information supplied by the user relating to test coverage predictions associated with specific functional blocks including the importing of component reference designator and pin number.

Manual importing of this type of data in the form of a MS Excel spreadsheet is prone to human error, which often results in incorrect information being entered.

Figure 6



A	B	C	D	I	J	K	L
ref	type	complexity	pin_cnt	coverage_presence	coverage_polarity	coverage_value	coverage_solder
2	R96	680R	RLC	2	100.0	100.0	100.00
3	R97	680R	RLC	2	100.0	100.0	100.00
4	R98	1K	RLC	2	100.0	100.0	100.00
5	R99	1K	RLC	2	100.0	100.0	100.00
6	A5	DISPLAY	SSI/MSI	10	100.0	100.0	100.00
7	A6	DISPLAY	SSI/MSI	10	100.0	100.0	100.00
8	A7	DISPLAY	SSI/MSI	10	100.0	100.0	100.00
9	C1	4.7/10	RLC	2	100.0	100.0	100.00
10	C2	4.7/10	RLC	2	100.0	100.0	100.00
11	C3	4.7/10	RLC	2	100.0	100.0	100.00
12	C4	4.7/10	RLC	2	100.0	100.0	100.00

Subsequently, it was felt that these problems could be eliminated by utilizing schematic and layout viewers

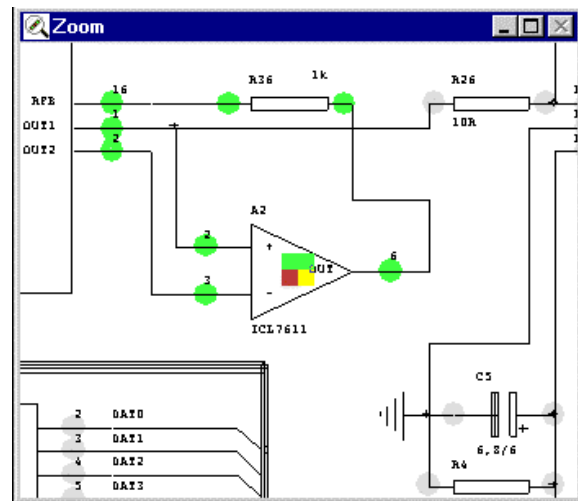
to select components within a functional block and attach a coverage value to each PPVS defect facet to reflect the level of defect coverage provided by specific tests as depicted in figure 6.

In the example shown, resistor R99 has been highlighted within the schematic viewer and allocated the following PPVS coverage values:

- [P] component presence = 100%
- [P] component polarity = 100%
- [V] component value = 0.0%
- [S] component solder = 100%

PPVS fault coverage predictions can either be made for each selected component or by pin. At the component level each PPVS facet is allocated a color code depending upon the level of fault coverage provided by each specific test.

Figure 7



In the above example the PPVS icon represents the fault coverage for component A2 in respect to the PPVS criteria, with each pin also declared as having 100% coverage as indicated by the green circles.

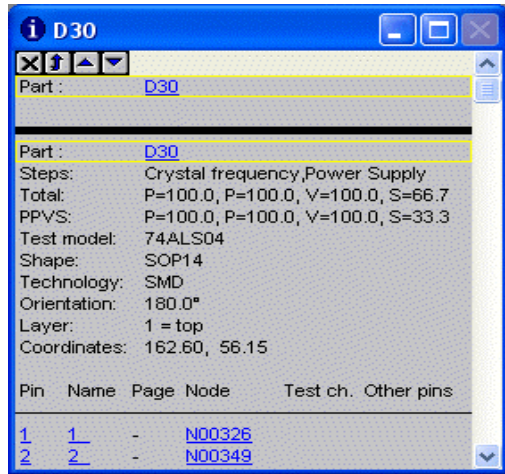
The PPVS color coding for device A2 indicates the following declarations:



- Presence: 100%
- Polarity: 100%
- Value: 0%
- Solder: 60%

This can be expanded to provide more detailed information relating to coverage predictions for specific functional test steps as shown.

Figure 8



Initially, all selected devices inherit 100% coverage for each of the Presence, Polarity and Value facets. The coverage figure could be graphically updated to reflect customer estimation. The Solder coverage is computed, based on the number of covered pins divided by the total number of device pins.

Declaration by test steps allows:

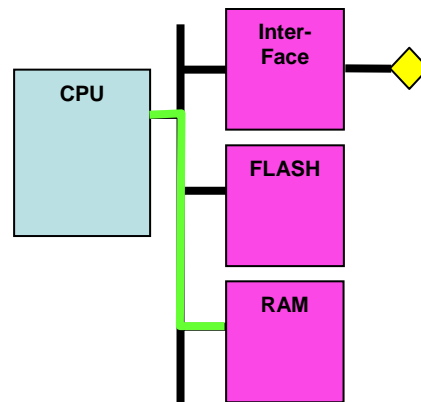
- A cross-analysis between the test coverage declaration and the functional tester transcript log file will confirm that all the test steps are really implemented within the test program.
- If a test step passes, it identifies the functional area that is free of defects, so if a test step subsequently fails that includes an already tested component; the 'Sherlock algorithm' can identify the most probable source of failure.

4.2 Deduction Method

The **Deduction** method makes a prediction based upon the premise that certain components within a functional block are covered by specific test sequences, e.g. a memory block functional test will exercise the majority of the pins on the memory device and a percentage of the pins on the interconnecting microprocessor.

The requirements for any functional test step can be declared within product specific or generic rule based models. These can be relatively simple rules described in ASCII text that search for certain criteria within a design netlist e.g. are the pins of device class 'RAM' connected to the pins of device class 'PROCESSOR' etc.

Figure 9



Alternatively, an at-speed loop-back test between interconnecting high-speed, LVDS serial communication links will prove the embedded serialization (parallel-to-serial conversation) capability of the transmission device(s) and receiving device(s), and the PPVS coverage of any other components included within the loop-back test.

The formal language limits any inconsistency in the declaration. When you describe the test vector flow during the test, you are sure that all the pins on the net will be declared as involved in the test (no missing declaration).

The deduction method can manage multiple instances of similar connection properties, using some form of low level test reuse described in a formal rule, which could be applied on different component/pins.

However, when the communication protocol becomes more complex, or when there are prerequisites for the test step, it becomes far too complex to describe the test. Subsequently, the deduction method is typically used where board complexity is relatively simple i.e. the automotive industry.

As the complexity increases, the **inheritance** method is the preferred solution.

4.3 Inheritance Method

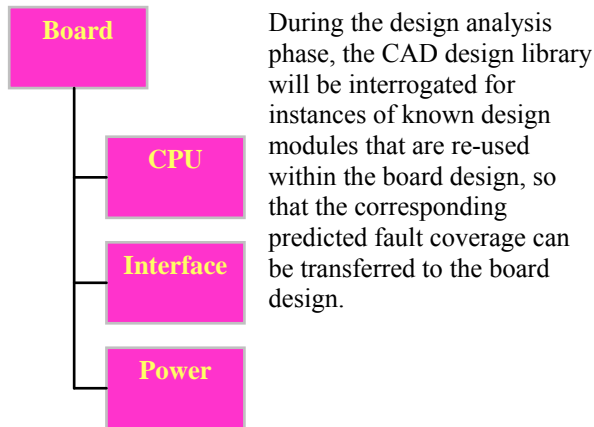
The **Inheritance** method can be utilized to re-use test coverage predictions associated with functional blocks within a design.

This is particular useful within hierarchical design flows that reuse several instances of the same modules/functions, where information can be transferred to multiple instances of the functional block and thus eliminating the need to reproduce the fault coverage predictions for every instance of the design re-use.

This is possible by associating partlist and netlist information with predicted functional test fault coverage figures, so that:

- The module description can either be exported from a CAD module library or extracted from an existing board schematic,
- The functional test coverage details can be supplied manually, from a fault simulator, or by using the TestWay **declaration** or **deduction** methods.

Figure 10



The module matcher checks if a known module corresponds to a subset of the board.

The module connectivity is compared with the board connectivity and computes a matching percentage between the module and a subset of the board.

When the matching percentage equals 100%, the module test coverage is transferred to the board.

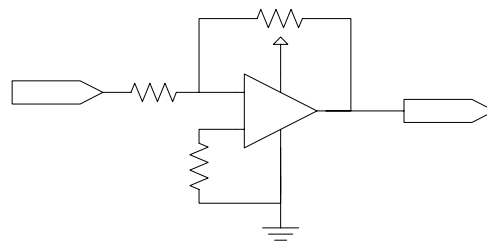
In order to recognize/match a module/function, we use the following module/function information:

1. Component reference designator
2. Component type or component function
3. Pin number
4. Net name

[1] and [2] are linked with the component; [3] and [4] are linked with connectivity.

When the module/function is instantiated more than once, reference designator [1] and net name [4] are updated automatically by the CAD design tool. Under these circumstances, it is clear that the module matcher can't use the reference designator [1] and net name [4] and should only use component type [2] and pin number [3].

Figure 11



The current implementation of the module matcher makes it possible to properly manage variations in design instances that have identical functionality, such as:

- Resistor R1 could be mounted reverse (swapping between pin 1 and pin2),
- The resistors (R1, R2 & R3) could be packed in a resistor array. In this case, even component type [2] and pin number [3] become irrelevant.
- Connector pins (P1-A1 or P1-A2) could be handled differently in either of the following cases:
 - a) When it is mandatory to use a certain pin only (standard connector).
 - b) The function is still the same even if a pin is connected to another connector point.
- Optional components: Some module components are optional. For example DNP components may be missing on a board, but the function is still the same.

The recent improvement is linked with the Variant management on PCB and on modules:

- A PCB design could be instantiated with multiple variants. Some CAD systems provide features to handle multiple variants on one board within a single design project.
- In this context, each module could have variants. Each variant could be associated with a different coverage.

To achieve a realistic Design for Test analysis of hierarchical designs, it is important to work closely with EDA companies, to become an integral part the standard design and test flow in order to handle the coverage variance within single design projects. This is the real meaning of "Design for Test"?

The inheritance approach is not limited to functional test coverage only:

- It can be used for sophisticated clusters, combining boundary-scan and emulation, and
- Where emulation is used as a test strategy⁷, the inheritance approach can analyze the design hierarchy and pass the coverage variance information to COTS based emulation tools.

5 Combining Test Strategies

Functional test fault coverage estimations can be used in conjunction with coverage estimations provided by complimentary test strategies such as Automated Optical Inspection (AOI); Automated X-ray Inspection (AXI); In-Circuit test (ICT); Flying Probe test (FPT); Boundary-Scan test (BST) and Functional test (FT) to provide a total fault coverage estimation for the board.

From the complete information database it is possible to determine components that are not covered, but also optimize the overall test strategy to ensure that there is no overlap in the fault coverage provided by tests. This allows the correct balance to be maintained between test time and diagnostic accuracy.

The information contained within the fault coverage database can also be utilized to fine tune the test strategy and eliminate any redundant test processes.

It also allows test engineering groups to examine the overall test strategy; so that functional tests can focus

on areas where structural test coverage is prohibitive i.e. under RF shielding where physical test access and inspection techniques are not possible.

Alternatively, the combined fault coverage of several boards can be correlated to provide an estimated system level test coverage figure.

6 Conclusions

Technological development produces new problems that call for new tools. Test coverage estimation is one of these tools. From design, during production, and in a more general way, through the whole product life cycle, coverage estimation permits the test process to be optimized.

In assessing the results from a combination of test methods it is possible to simulate a variety of test strategies and predict the relative fault coverage⁶. By deploying various testers in the optimum order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels improved.

The economic challenges are critical; the tools to meet them are available.

7 References

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